**SWISSDIS** 



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# **SPECIFICATIONS**

# **SD1021-V00**

Swissdis 107997

LCD Module Graphic 128x64 Dots With LED Backlight white

Version February 2012

Revision	Revision Date	Page	Contents
Α	2011/11/25		Initial Release and Issue Full Specification.



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#### 1. FEATURES

The features of LCD are as follows

\* Display mode : FSTN, Positive, Transflective

\* Color : Display dot : White

Background: Black

\* Display Format : 128 Dots × 64 Dots graphic

\* IC : Sitronix ST7565P-G

\* Interface Input Data : Parallel and Serial Interface MPU

\* Driving Method : 1/65 Duty, 1/9 Bias

\* Viewing Direction : 12 O'clock

\* Backlight : LED(White)

\* LCM technological conditions: **RoHS** 

#### 2. MECHANICAL SPECIFICATIONS

Item	Specification	Unit
Module Size	54.6(W) X 42.2(H) X 4.48MAX(T)	mm
Viewing Area	50.6MIN(W) X 31.0MIN(H)	mm
Effective Display Area	46.577(W) X 27.697(H)	mm
Number of Dots	128 X 64 Dots	-
Dot Size	0.349(W) X 0.418(H)	mm
Dot Pitch	0.364(W) X 0.433(H)	mm

#### 3. ELECTRICAL SPECIFICATIONS

#### 3-1. Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Sta			
item	Зуппоп	Min.	Тур.	Max.	Unit
Supply Voltage For Logic	VDD	0.3	-	5.0	V
Supply Voltage For LCD Drive	Vo, Vout	0.3	-	18.0	V
Operating Temp.	Тор	0	-	+50	°C
Storage Temp.	Tst	-20	-	+65	°C
Static Electricity	Be sue th	at you are	ground wh	en handinç	g LCM

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## 3. ELECTRICAL SPECIFICATIONS (Continued)

#### 3-2. Electrical Characteristics

Item		Symbol	Test Condition	Min.	Тур.	Max.	Unit
Supply Voltage For Logic		VDD - VSS	-	3.0	3.3	3.6	V
Supply Voltage For LCD		V0-Vss	Ta=25°ℂ	9.20	9.50	9.80	V
	"H" Level	V <sub>IH</sub>		0.8V <sub>DD</sub>	-	VDD	V
Input Voltage	"L" Level	V <sub>IL</sub>	-	Vss	-	0.2VDD	V
Output Voltage	"H" Level	V <sub>OH</sub>	I <sub>OUT</sub> = -0.5mA	0.8V <sub>DD</sub>	-	VDD	V
Output Voltage	"L" Level	V <sub>OL</sub>	I <sub>OUT</sub> = 0.5mA	Vss	-	0.2VDD	V
Current Consumption		I <sub>DD</sub>	$V_{IN} = V_{DD}$	-	0.50	2.0	mA

NOTE: 1) Duty ratio=1/65, Bias=1/9

2) Measured in Dots ON-state

## 3-3. Backlight

## 3-3-1. Absolute Maximum Ratings at Ta=25 $^{\circ}\!\!\!\subset$

Item	Symbol	Rating	Unit
Peak Forward Current	IFP	2*40	mA
Reverse Voltage	Vr	5	V
Power Dissipation	Pd	2*156	mW
Storage Temperature Range	Tstg	-20~+65	$^{\circ}\!\mathbb{C}$
Hand Soldering Temperature	<b>350</b> ℃	-	

## 3-3-2. Electronic Optical Characteristics (If=2\*30mA)

Item	Symbol	Min.	Тур.	Max	Unit
Forward Voltage	VF	3.3	3.6	3.9	V
Luminous Intensity	lv	800	-	-	cd/m <sup>2</sup>
Uniformity	U	70	-	-	%
AVG. X OF 1931 C.I.E	Х	0.27	0.30	0.33	-
AVG. Y OF 1931 C.I.E	Y	0.27	0.30	0.33	-

<sup>\*</sup> The brightness is measured without LCD panel

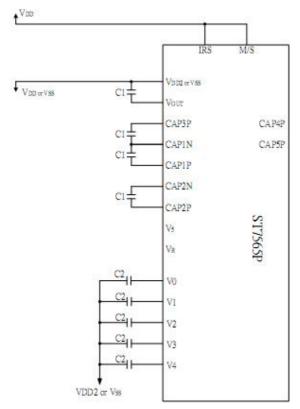
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#### 4. POWER SUPPLY and BLOCK DIAGRMA

#### 4-1 Power supply

When the voltage regulator internal resistor is not used.

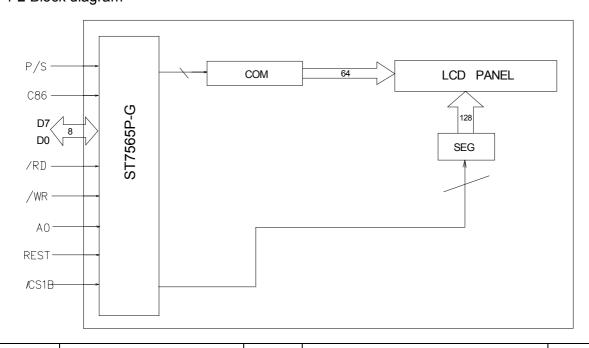
(Example where VDD2=VDD, with 4x step-up)



## 4-2 Block diagram

**MODEL** 

SD1021-V00



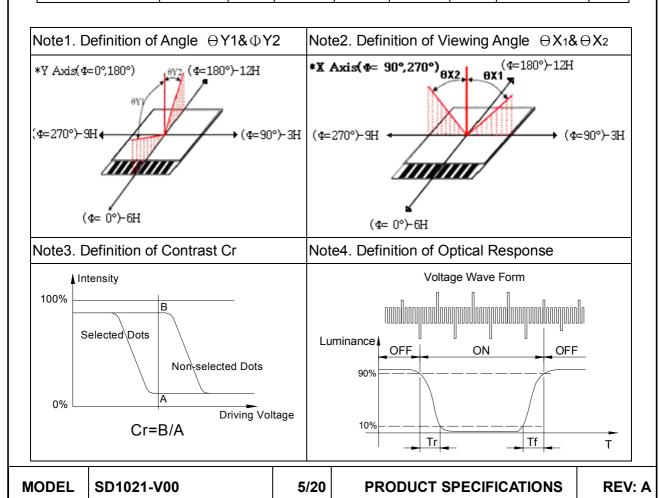
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#### 5. ELECTRO - OPTICAL CHARACTERISTICS

Ite	m	Symbol	Temp.	Min.	Тур.	Max.	Unit	Conditions	Note
	Ф=0°	⊕1			30				
Viewing	Ф=180°	⊖2	<b>25</b> ℃		33		Dog		1.0
Angle Cr <u>&gt;</u> 2	Ф=90°	⊖3	250		28		Deg.	-	1,2
	Ф=270°	⊖4			30				
Viewing Direction						12 O'clo	ck		
Cont Rat		Cr	25℃	2.0	4.68	4.98	-	$ \Phi = 0^{\circ} $	3
Respo	Response Tr		<b>25</b> ℃	-	108	300	ms	⊖= 0°	4
Time(rise)	11	0℃	-	950	1150	1113	$\Phi$ = 0°	_	
Respo	onse	Tf	<b>25</b> ℃	-	228	300	me	⊖= 0°	4
Time	(fall)	11	0℃	-	950	1150	ms	$\Phi$ = 0°	+



## **6. INTERFACE PIN FUNCTION**

Pin NO.	Symbol	1/0	Functions
1	P/S	I	This pin configures the interface to be paraller mode or serial mode. P/S="H":Parallel data input/output; P/S="L":Serial data input.
2	C68	I	This is the MPU interface selection pin.C86="H":6800 Series MPU interface; C86="L":8080Series MPU interface.
3~7	V0~V4	Power Supply	This is a multi-level power supply for the liquid crystal drive.
8	C2-	0	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
9	C2+	0	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
10	C1+	0	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
11	C1-	0	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
12	C3+	0	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
13	VOUT	0	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD
14	VSS	Power Supply	Ground
15	VDD	Power Supply	Power supply
16~23	D7~D0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
24	/RD	ı	When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L". When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.

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## 6. INTERFACE PIN FUNCTION (Continued)

Pin NO.	Symbol	1/0	Functions
25	WR	I	When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type: When R/W="H": Read; When R/W="L": Write.
26	A0	I	This terminal selects the resistors for the V0 voltage level adjustment.
27	REST	I	When REST is set to "L", the setting are initialized.
28	/CS1B	I	This is the chip select signal.When/CS1B="L", then the chip select becomes active, and data/command I/o is enabled
29	Anode1	Power	Backlight Anode (A1+)
30	Cathode1	Power	Backlight Cathode (K1-)
31	Anode2	Power	Backlight Anode (A2+)
32	Cathode2	Power	Backlight Cathode (K2-)

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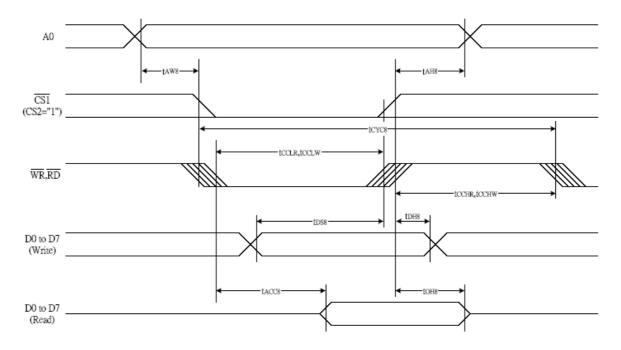
## 7. COMMAND LIST

Command	85		- 0		nma			_				Function
	A0	/RD	/WR							-	D0	42.77
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	D	ispla	ay st	art a	addr	ess	Sets the display RAM display star line address
(3) Page address set	0	1	0	1	0	1	1	Pa	ige :	addi	ess	Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Mo	st si	gnif	icant	Sets the most significant 4 bits of
Column address set lower bit	0	1	0	0	0	0	0	Lea	ast s	igni	ficant dress	the display RAM column address Sets the least significant 4 bits of the display RAM column address
(5) Status read	0	0	1		St	atus	3	0	0	0	0	Reads the status data
(6) Display data write	1	1	0			d	Writ	e da	ta			Writes to the display RAM
(7) Display data read	1	0	1			3	Rea	d da	ita			Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON
(11) LCD blas set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	•		٠	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1		pera	iting	Select internal power supply operating mode
(17) Vo voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0		esis atio	tor	Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0			0 nic v	_		1 value	Set the Vo output voltage electronic volume register
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	0: OFF, 1: ON
Static indicator register set	5	χō		0	0	0	0	0	0	0		Set the flashing mode
(20) Boosterratio set	0	1	0	1	1		1 0			ste	0 ep-up alue	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver	8)											Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1		. ¥		٠	Command for IC test. Do not use this command

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#### 8. TIMING CHARACTERISTICS

#### 8-1. 8080 Series MPU



(VDD = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rati	ing	Units
item	Signal	Symbol	Condition	Min.	Max.	Ullits
Address hold time		tah8		0	–	
Address setup time	A0	taws		0	_	]
System cycle time		tcycs		240	_	]
Enable L pulse width (WRITE)	WR -	tccLw		80	_	]
Enable H pulse width (WRITE)		tccнw		80	_	]
Enable L pulse width (READ)	RD	tcclr		140	_	Ns
Enable H pulse width (READ)	, KD	tcchr		80		]
WRITE Data setup time		toss		40	_	]
WRITE Address hold time	D0 to D7	tDH8		0	_	]
READ access time		taccs	CL = 100 pF	_	70	]
READ Output disable time		tонв	CL = 100 pF	5	50	

<sup>\*1</sup> The input signal rise time and fall time  $(t_r, t_r)$  is specified at 15 ns or less. When the system cycle time is extremely fast,  $(t_r + t_r) \le (t_{CYCS} - t_{CCLW} - t_{CCLW})$  for  $(t_r + t_r) \le (t_{CYCS} - t_{CCLW})$  are specified.

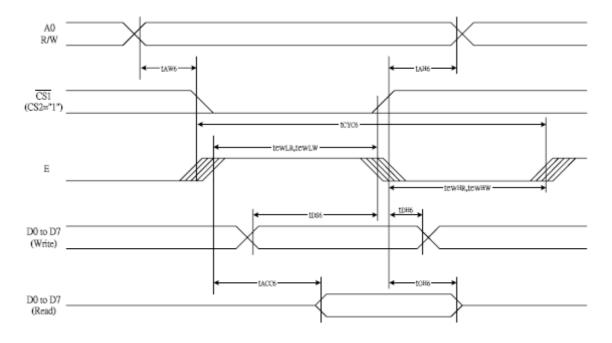
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<sup>\*2</sup> All timing is specified using 20% and 80% of  $\forall \text{od}$  as the reference.

<sup>\*3</sup> tccLw and tccLR are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

## **8. TIMING CHARACTERISTICS (Continued)**

#### 8-2. 6800-Series MPU



(VDD = 3.3 V , Ta = 25°C )

				(**************************************	v , ra – 25	$\sim$ $_{-}$
Item	Signal	Symbol	Condition	Rat	ing	Units
item	Signal	Symbol	Condition	Min.	Max.	Offics
Address hold time		tan6		0	_	
Address setup time	A0	taw6		0	_	
System cycle time		tcyc6		240	_	
Enable L pulse width (WRITE)	WR	tewuw		80	_	
Enable H pulse width (WRITE)	WIX	tewnw		80	_	
Enable L pulse width (READ)	RD	tewlr		80	_	ns
Enable H pulse width (READ)	, KD	tewnr		140		
WRITE Data setup time		tos6		40	_	]
WRITE Address hold time	D0 to D7	t <sub>DH6</sub>		0	_	]
READ access time	D0 to D7	tacc6	CL = 100 pF	_	70	]
READ Output disable time	]	toн6	CL = 100 pF	5	50	]
		•				_

<sup>\*1</sup> The input signal rise time and fall time (tr, tr) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tr) ≤ (tcγcs – tewnw – tewnw) for (tr + tr) ≤ (tcγcs – tewnw – tewnw) are specified.

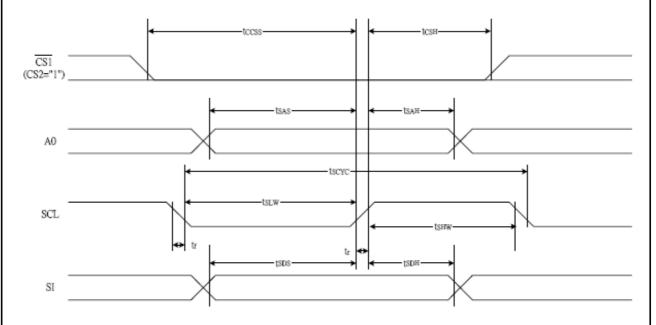
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<sup>\*2</sup> All timing is specified using 20% and 80% of Voo as the reference.

<sup>\*3</sup> tewsw and tewsr are specified as the overlap between CS1 being "L" (CS2 = "H") and E.

## 8. TIMING CHARACTERISTICS (Continued)

#### 8-3. The Serial Interface



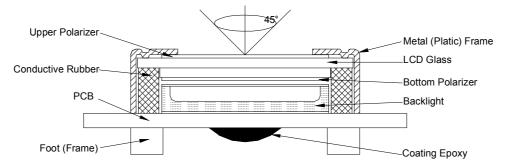
(Vpp = 3.3V, Ta =25°C)

				(**************************************	37, TG -23	
Item	Signal	Symbol	Condition	Rat	Rating	
nem	Sigilal	Symbol	Condition	Min.	Max.	Units
Serial Clock Period		Tscyc		50	_	
SCL "H" pulse width	SCL	Tshw		25	_	
SCL "L" pulse width		Tstw		25	_	7
Address setup time	40	Tsas		20	_	
Address hold time	A0	Tsah		10	_	ns
Data setup time	C.I.	Tsds		20	_	
Data hold time	SI	Тѕон		10	_	7
CS-SCL time	06	Тсьь		20	_	
CS-SCL time	cs	Tosh		40	_	]

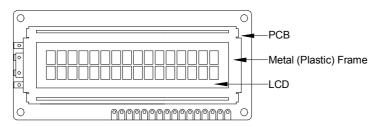
<sup>\*1</sup> The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
\*2 All timing is specified using 20% and 80% of Voo as the standard.

#### 9. QUALITY SPECIFICATION

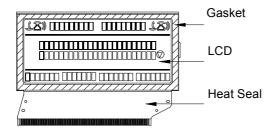
- 9 1. LCM Appearance and Electric inspection Condition
  - 1. Inspection will be done by placing LCM 30cm away from inspector's eyeballs under normal illumination.



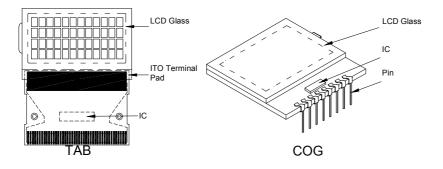
- 2. View Angle: with in 45° around perpendicular line.
- 9 2. Definition
  - 1. COB



2. Heat Seal



3. TAB and COG



## 9. QUALITY SPECIFICATION (Continued)

9-3. Sampling Plan and Acceptance

1.Sampling Plan

MIL - STD - 105E (  $\parallel$  ) ordinary single inspection is used.

2.Acceptance

Major defect: AQL = 0.25Minor defect: AQL = 0.65

9-4. Criteria

#### 1.COB

Defect	Inspection Item	Inspection Standards	
Major	PCB copper flakes peeling off	Any copper flake in viewing Area should be greater than 1.0mm <sup>2</sup>	Reject
Major	Height of coating epoxy	Exceed the dimension of drawing	Reject
Major	Void or hole of coating epoxy	Expose bonding wire or IC	Reject
Major	PCB cutting defect	Exceed the dimension of drawing	Reject

#### 2.SMT

Defect	Inspection Item	Inspection Standa	ards
Minor	Component marking not readable		Reject
Minor	Component height	Exceed the dimension Of drawing	Reject
Major	Component solder defect (missing, extra, wrong component or wrong orientation		Reject
Minor	Component position shift  component soldering pad  X  D  Z  Y	X < 3/4Z Y > 1/3D	Reject Reject
Minor	Component tilt component soldering pad	Y > 1/3D	Reject
Minor	Insufficient solder component PAD PCB	<i>θ</i> ≤ 20°	Reject

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## 9. QUALITY SECIFICATION (Continued)

9-4. Criteria (Continued)

3. Metal (Plastic) Frame

Defect	Inspection Item	Inspection Standards				
Major	Crack / breakage	Anywhere	Reject			
		W	L	Acceptable of Scratch		
		w<0.03mm	Any	Ignore		
		0.03mm <u>&lt;</u> w<0.05mm	L <u>&lt;</u> 5.0mm	2		
Minor	Frame Scratch	0.05mm <u>&lt;</u> w<0.1mm	L <u>&lt;</u> 3.0mm	1		
		w <u>&gt;</u> 0.1mm	Any	0		
		Note: 1. Above criteria applicable to scratch lines wit distance greater than 5mm.  2. Scratch on the back side of frame (not visible) can be ignored.				
				Acceptable of Dents / Pricks		
		Φ <b>≤</b> 1.0mr	n	2		
	Frame Dent, Prick	1.0<⊕ <u>&lt;</u> 1.5ı	1			
Minor	$\Phi = \frac{L + W}{2}$	1.5mm>(	0			
	2	Note: 1. Above criteria applicable to any two dents / pricks with distance greater than 5mm 2. Dent / prick on the back side of frame (not visible) can be ignored				
Minor	Frame Deformation	Exceed the dimension of drawing				
Minor	Metal Frame Oxidation		Any rust			

## 4. Flexible Film Connector (FFC)

Defect	Insp	ection Item	Inspection Standards				
Minor	Tilte	d soldering	Within the angle ±3°	Acceptable			
Minor	Uneven s	older joint /bump		Reject			
Minor	Hole	Φ= <u>L+W</u>	Expose the conductive line	Reject			
IVIII IOI	Tiole	$\Psi^{-}$ 2	→ > 1.0mm	Reject			
Minor	Position shift		Y > 1/3D	Reject			
MINO	**************************************	<u></u>	X > 1/2Z	Reject			

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## 9. QUALITY SPECIFICATION (Continued)

## 9-4. Criteria (Continued)

#### 5. Screw

Defect	Inspection Item	Inspection Standards	
Major	Screw missing/loosen		Reject
Minor	Screw oxidation	Any rust	Reject
Minor	Screw deformation	Difficult to accept screw driver	Reject

## 6. Heat seal . TCP . FPC

Defect	Inspection Item	Inspection Standards	
Major	Scratch expose conductive layer		Reject
Minor	HS Hole $\Phi = \frac{L + W}{2}$	Ф> 0.2mm	Reject
Major	Adhesion strength	Less than the specification	Reject
Minor	Position shift	Y > 1/3D	Reject
IVIII IOI	X		Reject
Major	Conductive line break		Reject

## 7. LED Backing Protective Film and Others

Defect	Inspection Item	Inspection Standards					
		Acceptable number of units					
		Ф <u>&lt;</u> 0.10mm	Ignore				
		0.10<⊕ <u>&lt;</u> 0.15mm	2				
Minor	LED dirty, prick	0.15<⊕ <u>&lt;</u> 0.2mm	1				
		Φ>0.2mm	0				
		The distance between any two spots should be ≥ Any spot/dot/void outside of viewing area is accept					
Minor	Protective film tilt	Not fully cover LCD	Reject				
Major	COG coating	Not fully cover ITO circuit	Reject				

## 8. Electric Inspection

Defect	Inspection Item	Inspection Standards	
Major	Short		Reject
Major	Open		Reject

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## 9. QUALITY SPECIFICATION (Continued)

- 9-4. Criteria (Continued)
- 9. Inspection Specification of LCD

Defect	Insp	pect Item	Inspection Standards						s	
		* Glass Scratch	W	W <u>&lt;</u> 0.03			0.0	3 <w<u>&lt;0.0</w<u>	5 \	N>0.05
		* Polarizer Scratch	L	L<5				L<3		Any
Minor	Linear Defect	* Fiber and Linear	ACC. NO.	1			1		Reject	
		material	Note	L is the length and W is the				width of	the de	efect
		* Foreign material	Φ	Φ.	<u>&lt;</u> 0.1	0.1<Ф<	0.15	0.15<⊕	<0.2	Ф>0.2
		between glass and polarizer or glass	ACC. NO.	3EA	/1PC	2		1		0
Minor	Polarizer Pricked	and glass  * Polarizer hole or protuberance by external force	Note			•		of the de ects > 10m		
		* Unobvious	Φ	Φ<	<u>&lt;</u> .1	0.1<⊕ <u>&lt;</u>	0.15	0.15<⊕	<u>&lt;</u> 0.2	Ф>0.2
	White Spot	transparant foreign material between	ACC. NO.	3EA /	1PC	2		1		0
Minor	and Bubble in polarizer	glass and glass or glass and polarizer * Air protuberance between polarizer and glass	Note		$\Phi$ is the average diameter of the defect. Distance between two defects > 10mm.					
			Φ	Φ <u>&lt;</u> 0.10 0.10			0<Φ <u>&lt;</u> 0.20			⊕>0.2
		<u></u>	ACC. NO.	3EA /	EA /1PC		2			0
Minor	Segment Defect	· W		W is more than 1/2 segment width Reject				Reject		
			Note	$\Phi = \frac{L + W}{2}$ Distance between two defect is 10mm						
			Φ	Φ<	0.10	0.	10<	0 <u>&lt;</u> 0.20		Ф>0.2
Minor	Protuberant Segment		W	G	Glue		W <u>&lt;</u> 1/2 Seg , W <u>&lt;</u> 0.2			Ignore
	Ocginent	Φ = ( L + W ) / 2	ACC. NO.	3EA /1PC			2 0			0
			1. Seg	ment						
			Е	3	B<0.	4mm (	).4 <b< td=""><td>&lt;1.0mm</td><td>B&gt;</td><td>1.0mm</td></b<>	<1.0mm	B>	1.0mm
	<b>A</b> 11		B-	A	B-A<	<1/2B	B-A	_ \<0.2	B-A	\<0.25
Minor	Assembly Mis-alignment	HB-1 -1 F-A	Jud	lge	ge Accepta		otable Acceptable		Acceptable	
	iviis-aligi IIII EIIL	175	2. Dot	Matrix						
				Deformation>0.35mm					Reject	
Minor	Stain on LCD Panel Surface		or a	similar	one.	Otherwis	se, ju	d lightly w idged acc hite Spot"		

MODEL	SD1021-V00	16/20	PRODUCT SPECIFICATIONS	REV: A
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## 10. RELIABILITY

NO.	ltem	Condition	Criterion		
1	High Temperature Operating	70℃, 96Hrs			
2	Low Temperature Operating	-20°ℂ, 96Hrs			
3	High Humidity	60°C, 90%RH, 96Hrs			
4	High Temperature Storage	80°C, 96Hrs	No defect in cosmetic		
5	Low Temperature Storage	-30°C, 96Hrs	and operational function allowable.  Total current		
6	Vibration	Random wave  10 ~ 100Hz  Vibration  Acceleration: 2G  60 Minute			
7	Thermal Shock	-10°C to 25°C to 60°C  (60Min) (15Min) (60Min)  10Cycles			
o	ESD Testing	Contract Discharge Voltage: +1 ~ 5kV and –1 ~ –5kV	There will be discharged ten times at every discharging		
8	ESD lesting	Air Discharge Voltage: +1 ~ 8kV and –1 ~ -8kV	voltage gap is 1kV.		

Note:

- 1) Above conditions are suitable for Swissdis standard products.
- 2) For restrict products, the test conditions listed as above must be revised.

#### 11. HANDLING PRECAUTION

(1) Mounting Method

The panel of the LCD Module consists of two thin glass plates with polarizers which easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD Modules.

(2) Caution of LCD handling & cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichlorotrifloroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Ketone
- Aromatics
- (3) Caution against static charge

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

#### (4) Packaging

- Modules use LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
- To prevent modules from degradation. Do not operate or store them exposed directly to sunshine or high temperature/humidity.
- (5) Caution for operation
  - It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limit shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.

#### 11. HANDLING PRECAUTION (Continued)

 Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them.

However those phenomena do not mean malfunction or out of order with LCD's. Which will come back in the specified operating temperature range.

- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the relative condition of 40°C, 80%RH or less is required.

#### (6) Storage

In the case of storing for a long period of time (for instance ,for years) for the purpose or replacement use, The following ways are recommended.

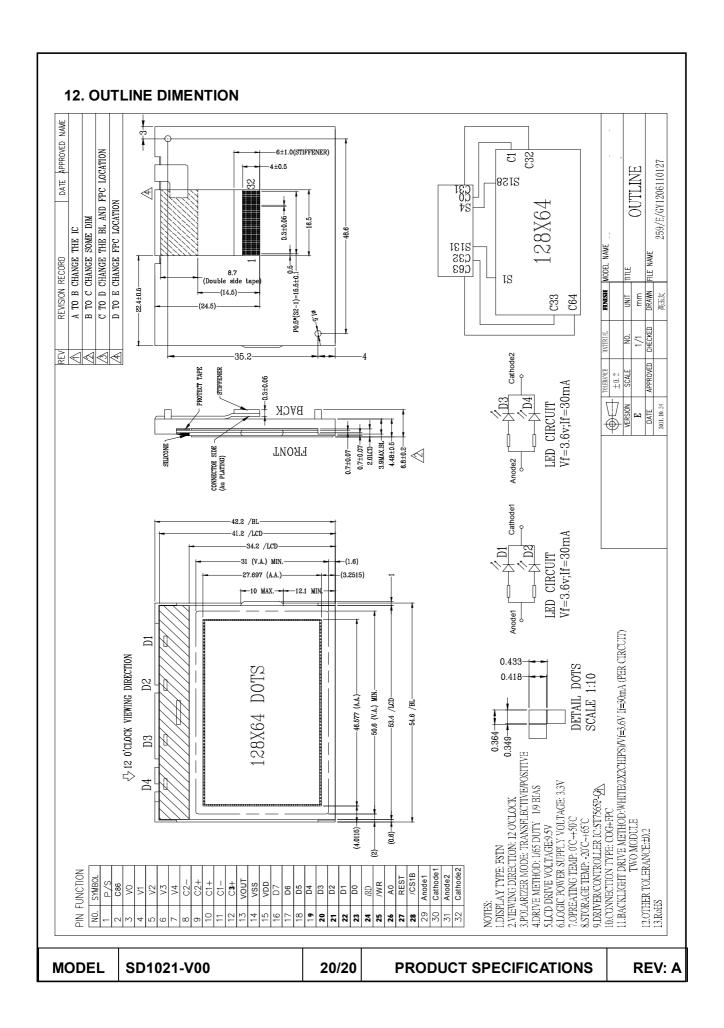
- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it, And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping temperature in the specified storage temperature range.
- Storing with no touch on polarizer surface by the anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery)

#### (7) Safety

 It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol.

Which should be burned up later.

- When any liquid crystal leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.



# SAMPLE OUTGOING INSPECTION REPORT (LCM)

Data: 2011/11/25 NO.: QAB11023

Cus	stomer		Pro	duct NO. Driving Voltage Testin					g Condition Quanti			Quantity		
Swis	ssdis AG	SD1021-V00					VOP: 9.5V				25℃ 10PCS			10PCS
Inspection Result														
lt	tems	Specification												
Displ	ay Mode	•	W/B	Mode	ОВ	/W M	ode	C	Yellow	Mode	○ E	Blue Mode		Gray Mode
Polar	izer Type	$\bigcirc$	Reflecti	ve			•	Tra	nsflective	)		○ Transm	nissive	e
	ewing ection	0	3 O'clod	ck	C	6 O'c	clock		0	9 O'cloc	k	•	12 O	o'clock
Electrical / Appearance														
I	ltem		Inspe	ection N	Method	I		;	Specifica	ation		Insp	ectio	n Result
App	earance		Spot	Gauge	Caliper		Final Inspection Criteri			n Criteria	a	• OK ○ N		
Ele	ectrical		L	.CM Tes	ster		Product Specification			cification		• OI	K	○ NG
Pa	attern		L	.CM Tes	ster		Drawing				• OI	K	○ NG	
					[	Dimens	sion /	Su	pply Cur	rent				
Item	Spec.(m	m)	NO.1	NO.2	NO.3	NO.4	NO	.5	Res	sult			Fig.	
L1	54.6 <u>+</u> 0.	2	54.63	54.72	54.60	54.60	54.6	31	● OK	○ NG				
L2	53.4 <u>+</u> 0.	2	53.32	53.32	53.42	53.32	53.3	39	● OK	O NG				
W1	42.2 <u>+</u> 0.	0.2 42.17		42.17	42.18	42.27	42.	19	● OK	O NG		4.003704	D O M O	
W2	41.2 <u>+</u> 0.	2	41.12	41.28	41.17	41.17	41.	12	• OK	○ NG	128X64		DOTS	FRONT  BACK E
Т	4.48 <u>+</u> 0.	.5	4.37	4.39	4.37	4.40	4.3	6	• OK	O NG				
IDD	2.0mA m	ax	0.50	0.50	0.50	0.50	0.5	0	• OK	O NG				
<b>Designed</b> ELIN			C	hecke	d		1		Ар	proved		Wallace		

Doc. NO.: F10018A